WHAT IS CLAIMED IS:

1. A driving circuit comprising:

a first transistor amplifier and a first current source, arranged in parallel with each other across an output terminal and a high potential power supply for charging said output terminal;

a second transistor amplifier and a second current source, arranged in parallel with each other across said output terminal and a low potential power supply for discharging said output terminal;

a driving period for driving said output terminal responsive to an input signal to a target voltage being made up by at least a first period and a second period; and

a control unit for performing control so that, in said first period, one of said first transistor amplifier and said second transistor amplifier is activated, with the other transistor amplifier being inactivated.

2. The driving circuit according to claim 1, wherein, during said first period, a first setting drive voltage of the output terminal, attained by charging by said first transistor amplifier, is lower than a second setting drive voltage of the output terminal, attained by discharging by said second transistor amplifier.

3. The driving circuit according to claim 1, wherein said current source, arranged parallel to say other transistor amplifier being inactivated is activated during said second period.

4. The driving circuit according to claim 1, further comprising:

a first differential circuit including a first differential pair, receiving input signal voltages from a non-inverting input terminal and

an inverting input terminal, as differential inputs, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier; and

a second differential circuit including a second differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

at least one of said first differential pair and the second differential pair being formed by a transistor pair with different threshold voltages.

5. The driving circuit according to claim 1, further comprising:

a first differential circuit including a first differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier;

a second differential circuit including a second differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

a plurality of transistors, connected parallel to each other, and having respective different threshold voltages, being provided as one transistor of a transistor pair forming at least one of said first and second

differential pairs; said plural transistors having control terminals connected in common to one of the non-inverting input terminal and the inverting input terminal which is different from the input terminal to which is connected the control terminal of the other transistor of the transistor pair forming said one differential pair; and

a control circuit for selecting at least one of said plural transistors as said one transistor of the transistor pair forming said one differential pair.

6. The driving circuit according to claim 1, further comprising:

a first differential circuit including a first differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier;

a second differential circuit including a second differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

a plurality of transistors, connected parallel to each other, and having respective different current driving capabilities, being provided as one transistor of a transistor pair forming at least one of said first and second differential pairs; said plural transistors having control terminals connected in common to one of the non-inverting input terminal and the inverting input terminal which is different from the input terminal to

which is connected the control terminal of the other transistor of the transistor pair forming said one differential pair;

a control circuit for selecting at least one of said plural transistors as said one transistor of the transistor pair forming said one differential pair.

7. The driving circuit according to claim 5, further comprising:

a plurality of switches for controlling on and off of the connection between said plural transistors and a load circuit for said one differential pair; and

a control circuit for controlling at least one of said switches so as to be turned on.

8. The driving circuit according to claim 1, further comprising:

a first differential circuit including a first differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, and a first load circuit connected to an output pair of said first differential pair, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier;

a second differential circuit including a second differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, and a second load circuit connected to an output pair of said second differential pair, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

at least one of said first load circuit and the second load circuit

being composed of a transistor pair formed by a pair of transistors having different threshold voltages.

9. The driving circuit according to claim 1, further comprising:

a first differential circuit including a first differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, and a first load circuit connected to an output pair of said first differential pair, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier;

a second differential circuit including a second differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, and a second load circuit connected to an output pair of said second differential pair, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

a plurality of transistors, connected parallel to each other, and having respective different threshold voltages, being provided as at least one transistor of the transistor pair forming at least one of said first and second load circuits; said plural transistors having control terminals connected in common to a control terminal of the other transistor of the transistor pair forming the one load circuit, or to both the control terminal of the other transistor and a connection node of one end of said one load circuit and the associated differential pair; and

a control circuit for activating at least one of the plural transistors.

10. The driving circuit according to claim 1, further comprising:

a first differential circuit including a first differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, and a first load circuit connected to an output pair of said first differential pair, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier;

a second differential circuit including a second differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, and a second load circuit connected to an output pair of said second differential pair, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

a plurality of transistors, connected parallel to one another, and having respective different current driving capabilities, being provided as at least one transistor of the transistor pair forming at least one of said first and second load circuits; said plural transistors having control terminals connected in common to a control terminal of the other transistor of the transistor pair forming the one load circuit, or to both the control terminal of the other transistor and a connection node of one end of said one load circuit and the associated differential pair; and

a control circuit for activating at least one of the plural transistors.

11. The driving circuit according to claim 1, further comprising:

a first differential circuit including a first differential pair,

receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, and a first load circuit connected to an output pair of said first differential pair, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier;

a second differential circuit including a second differential pair, receiving input signal voltages from a non-inverting input terminal and an inverting input terminal, as differential inputs, and a second load circuit connected to an output pair of said second differential pair, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

a plurality of resistors of different resistance values being provided to at least one of said first and second load circuits, as at least one of a resistor element of a resistor element pair forming said one load circuit; and

a control circuit for selecting at least one of said resistors and for connecting the selected resistor across an output of said differential pair associated with said one load circuit and the power supply associated with said one load circuit, as said one resistor element of the resistor element pair forming said one load circuit.

12. The driving circuit according to claim 1, further comprising:

a first switch connected in series with said first transistor amplifier across said high potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a second switch connected in series with said first current source

across said high potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a third switch connected in series with said second transistor amplifier across said low potential power supply and said output terminal and adapted to be turned on/off by a control signal; and

a fourth switch connected in series with said second current source across said low potential power supply and said output terminal and adapted to be turned on/off by a control signal.

13. The driving circuit according to claim 12, wherein

during said first period, said first and third switches are turned on and said second and fourth switches are turned off; and wherein

during said second period, said first and fourth switches are turned on and said second and third switches are turned off or said second and third switches are turned on and said first and fourth switches are turned off.

14. The driving circuit according to claim 1, further comprising

a switch provided across an input terminal and said output terminal and turned on/off by a control signal.

15. The driving circuit according to claim 1, further comprising:

a first switch connected in series with said first transistor amplifier across said high potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a second switch connected in series with said first current source across said high potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a third switch connected in series with said second transistor amplifier across said low potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a fourth switch connected in series with said second current source across said low potential power supply and said output terminal and adapted to be turned on/off by a control signal; and

a fifth switch connected across an input terminal and said output terminal and adapted to be controlled on/off by a control signal; wherein

the driving period for driving said output terminal to a target voltage further having a third period; wherein

during said first period, said first and third switches are turned on, said second and fourth switches are turned off and said fifth switch is turned off;

during said second period, said first and fourth switches are turned on, said second and third switch are turned off and said fifth switch is turned off, or

said second and third switches are turned on, said first and fourth switches are turned off and said fifth switch is turned off, and wherein

during said third period, said first to fourth switches are turned off and said fifth switch is turned on.

16. The driving circuit according to claim 1, further comprising:

a first differential circuit including a third current source connected to said low potential power supply, a first differential pair driven by said third current source and having a non-inverting input terminal and an inverting input terminal connected to an input terminal

and said output terminal, respectively, and a first load circuit connected across an output pair of said differential pair and said high potential power supply, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier;

a second differential circuit including a fourth current source connected to said high potential power supply, a second differential pair of the opposite conductivity type to the conductivity type of said first differential pair having a non-inverting input terminal and an inverting input terminal connected to an input terminal and to said output terminal, respectively, and a second load circuit connected across an output pair of said differential pair and said low potential power supply, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

a plurality of transistors, connected parallel to each other, and having respective different threshold voltages, being provided as one transistor of a transistor pair forming at least one of said first and second differential pairs; said plural transistors having control terminals connected in common to one of the non-inverting input terminal and the inverting input terminal which is different from the input terminal to which is connected the control terminal of the other transistor of the transistor pair forming said one differential pair;

a plurality of switches connected across said load circuit associated with said one differential pair and said current source driving said one differential pair, in series with each of said transistors, said switches being controlled on/off by a control signal; and

a control circuit for controlling at least one of said plural switches so as to be turned on during the driving period driving said output terminal to the target voltage.

17. The driving circuit according to claim 1, further comprising:

a first differential circuit including a third current source connected to said low potential power supply, a first differential pair driven by said third current source and having a non-inverting input terminal and an inverting input terminal connected to an input terminal and said output terminal, respectively, and a first load circuit connected across an output pair of said differential pair and said high potential power supply, an output of said first differential pair being supplied to a control terminal of said first transistor amplifier;

a second differential circuit including a fourth current source connected to said high potential power supply, a second differential pair of the opposite conductivity type to the conductivity type of said first differential pair, having a non-inverting input terminal and an inverting input terminal connected to an input terminal and to said output terminal, respectively, and a second load circuit connected across an output pair of said differential pair and said low potential power supply, an output of said second differential pair being supplied to a control terminal of said second transistor amplifier;

a plurality of transistors, connected parallel to each other, and having respective different current driving capabilities, being provided as one transistor of a transistor pair forming at least one of said first and second differential pairs; said plural transistors having control terminals

connected in common to one of the non-inverting input terminal and the inverting input terminal which is different from the input terminal to which is connected the control terminal of the other transistor of the transistor pair forming said one differential pair;

a plurality of switches connected across said load circuit associated with said one differential pair and said current source driving said one differential pair, in series with each of said transistors, said switches being controlled on/off by a control signal; and

a circuit for controlling at least one of said plural switches so as to be turned on during the driving period driving said output terminal to a target voltage.

18. The driving circuit according to claim 16, further comprising:

a first switch connected in series with said first transistor amplifier across said high potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a second switch connected in series with said first current source across said high potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a third switch connected in series with said second transistor amplifier across said low potential power supply and said output terminal and adapted to be turned on/off by a control signal; and

a fourth switch connected in series with said second current source across said low potential power supply and said output terminal and adapted to be turned on/off by a control signal.

19. The driving circuit according to claim 1, wherein

a first setting drive voltage of said output terminal, attained by charging by said first transistor amplifier, and a second setting drive voltage of said output terminal, attained by discharging by said second transistor amplifier, are set to respective different voltage levels with respect to an input level supplied to an input terminal; and wherein

a buffer area in which neither the first transistor amplifier nor the second transistor amplifier is in operation is provided between said first and second setting drive voltages.

20. The driving circuit according to claim 19, further comprising a circuit for performing control so that, during said first period, the first and second transistor amplifiers are both activatable, and so that, during said second period, one of said first transistor amplifier and the second transistor amplifier, responsible for driving for charging and driving for discharging, respectively, and the first current source or the second current source, performing the driving in the reverse direction to that of the one transistor amplifier, are both activated, to drive said output terminal to the target voltage.

21. The driving circuit according to claim 19, further comprising a circuit for controlling the setting of the range of said buffer area.

22. The driving circuit according to claim 21, wherein

said circuit for controlling the setting of the range of said buffer area includes:

a first differential circuit including a first differential pair of a first conductivity type, supplied with an input voltage supplied to said input terminal and with an output voltage at said output terminal from a non-

inverting input end and an inverting input end, respectively, to send a first signal from an output end to said first transistor amplifier; and

a second differential circuit supplied with an input voltage supplied to said input terminal and with an output voltage at said output terminal from a non-inverting input end and an inverting input end, respectively, to send a second signal from an output end to said second transistor amplifier; and wherein

at least during said first period, said first differential pair and/or said second differential pair are controlled so as to be formed by a transistor pair formed by a pair of transistors having respective different threshold voltages or different current driving capabilities.

23. The driving circuit according to claim 4, wherein the non-inverting input terminals of said first and second differential circuits are connected in common to an input terminal of the driving circuit and wherein the inverting input terminals thereof are connected in common to said output terminal.

24. The driving circuit according to claim 1, further comprising:

a first differential circuit including a first differential pair of a first conductivity type, receiving from a non-inverting input terminal and an inverting input terminal, an input voltage at said input terminal and an output voltage at said output terminal of said driving circuit, respectively and having an output terminal for supplying a first signal to said first transistor amplifier; and

a second differential circuit of a second conductivity type, receiving from a non-inverting input terminal and an inverting input terminal, an

input voltage at said input terminal and an output voltage at said output terminal, respectively, and having an output terminal for supplying a second signal to said second transistor amplifier;

at least one of said first differential pair and the second differential pair being formed by a transistor pair composed of a pair of transistors having respective different threshold values;

a first setting drive voltage of said output terminal, attained by charging by said first transistor amplifier, and a second setting drive voltage of said output terminal, attained by discharging by said second transistor amplifier, are set to respective different voltage levels with respect to an input level supplied to an input terminal;

a buffer area in which neither the first transistor amplifier nor the second transistor amplifier is in operation is provided between said first and second setting drive voltages; and wherein

when control is exercised during the second period of the driving period driving said output terminal to the target voltage, for activating said first transistor amplifier, activating said second constant current source and for inactivating both said second transistor amplifier and the first current source, the input voltage to said input terminal is supplied so that said first setting drive voltage is equal to said target voltage.

25. The driving circuit according to claim 24, wherein,

when control is exercised during the second period for activating said second transistor amplifier, activating said first current source and for inactivating both said first transistor amplifier and the second current source, the input voltage to said input terminal is supplied so that said

second setting drive voltage is equal to said target voltage.

26. A display apparatus comprising a plurality of data lines for supplying video signals to pixels of a display unit, and a driving circuit as set forth in claim 1 as a circuit for driving said data lines.

27. The driving circuit according to claim 6, further comprising:

a plurality of switches for controlling on and off of the connection between said plural transistors and a load circuit for said one differential pair; and

a control circuit for controlling at least one of said switches so as to be turned on.

28. The driving circuit according to claim 17, further comprising:

a first switch connected in series with said first transistor amplifier across said high potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a second switch connected in series with said first current source across said high potential power supply and said output terminal and adapted to be turned on/off by a control signal;

a third switch connected in series with said second transistor amplifier across said low potential power supply and said output terminal and adapted to be turned on/off by a control signal; and

a fourth switch connected in series with said second current source across said low potential power supply and said output terminal and adapted to be turned on/off by a control signal.